# System Planning for CoWoS and InFO Technologies

## Cadence Design Systems

# ABSTRACT

Design teams must now design entire systems, rather than each individual component of the system; no longer can the components of a system be designed in relative isolation. In this presentation, we'll introduce capabilities and flows that enable the designer to plan and optimize a system design in CoWoS or InFO that focuses on prototyping, planning and optimization of the constituent components, from IC IO pad ring design to system connectivity planning in a single, unified environment. We introduce a planning environment to address partitioning, placement, and net assignments which can transition from high level abstractions and a top-level netlist using best available data, then refine and optimize as detailed content emerges, and finally transition to the implementation tools for each component.

# System Planning for CoWoS and InFO Technologies

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TSMC OIP
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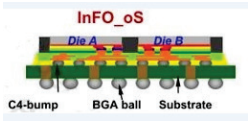
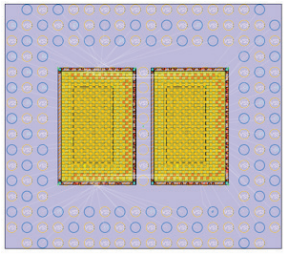
## "More than Moore" Impact on Cross-Platform Solutions

- Heterogeneous integration
  - Multi-PDK, multi-die module design (chips and chiplets)
  - Driven by IC layout platform for front-end design and multi-die layout back-end
- Merging IC back-end design with advanced IC packaging
  - Fan-out wafer-level packaging (FOWLP), 2.5D IC, and 3D IC (e.g. CoWoS and InFO)
- Cross-domain path finding and co-design
  - Pressure on cost vs. performance and time to market, coupled with many new packaging technologies means more time spent doing early cross-domain design tradeoffs
  - Over-the-wall approach to product design is obsolete
- Capacity
  - Multiple IC/FPGA cores on a single package/interposer = 1M pins
  - Complex metal balance requirements leading to millions of instances



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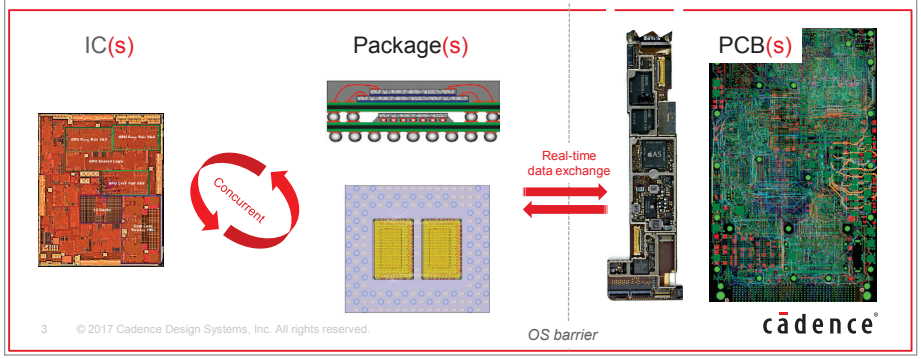
## Today's Design Challenges from an IC Package Designer's Perspective

- The explosion of advanced packaging multi-die technologies
  - WLP redefines packaging
    - Designed in package domain, verified and manufactured in IC domain
  - TSV driving 2.5D and 3D ICs
    - Multiple high-pin-count ICs (>250K) in single design and complex stacking
- Devices targeting multiple PCB form-factors with complex mechanical constraints
- Gigabit serial I/Os forcing cross-domain power *and* signal analysis of complete system

✓ ***Package designers now spend less than 50% of their time doing substrate layout***
  ✓ ***More time spent on planning/optimizing (path finding) across design domains***

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## So, What Is Path Finding?

- Early design assembly, planning, and optimization across adjacent design domains with the goal of increasing performance and lowering cost, while reducing time to market
  - Explore and tradeoff different package configurations and styles
  - Optimize ball-map assignments against multiple PCB form-factors
  - Analyze thermal and electrical effects across multiple assembly options
  - Prototype IC floorplans based on package/board level requirements
  - Plan and develop a BGA ball map based on PG ratios and rules
  - Customize BGA footprint
  - Target multiple package types for differing market segments
  - Package-level route feasibility studies
  - IC/package/PCB interconnect planning and optimization


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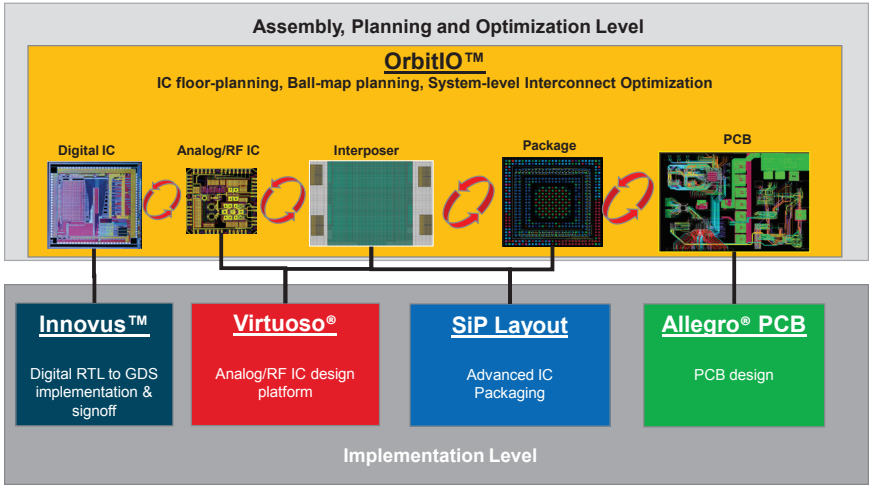
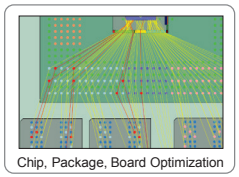
# OrbitIO Platform

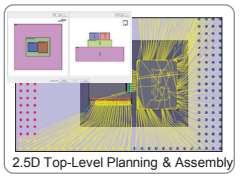
IC/interposer/package/PCB cross-domain planning and optimization

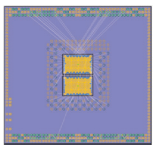


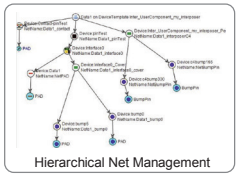

 

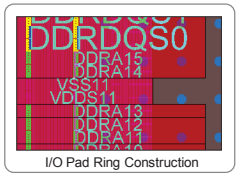
# OrbitIO Core Functionality (1)


Chip, Package, Board Optimization

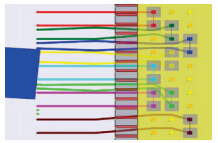

2.5D Top-Level Planning & Assembly


Multi-Die I/O Optimization


Hierarchical Net Management

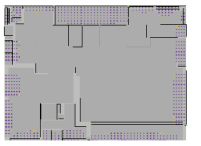


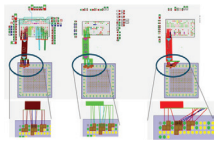
I/O Pad Ring Construction

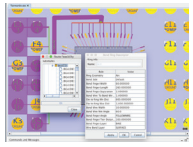

Breakout/Escape Routing

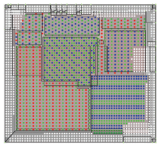
 

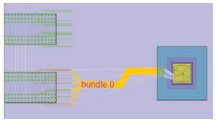
# OrbitIO Core Functionality (2)

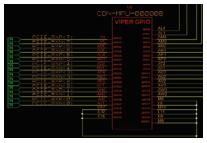

Rule Driven Signal I/O Bump Arrays


Design Variants


Bond Wire Planning & Optimization

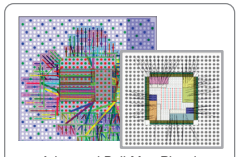

Advanced Core Bump Patterns

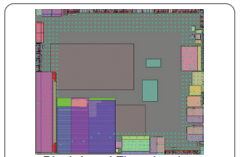

Bundle-Based Interconnect Planning

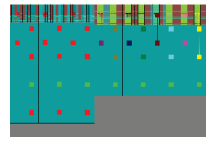

Board-Level Schematic Sync

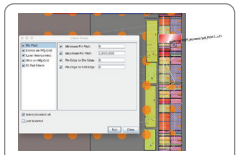
 

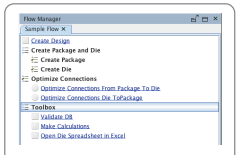
# OrbitIO Core Functionality (3)


Advanced Ball-Map Planning

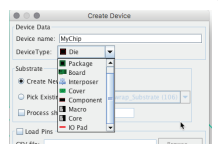

Block-Level Floorplanning


Tiling


DRC Checking



User Defined Flows



Start From Nothing Flow

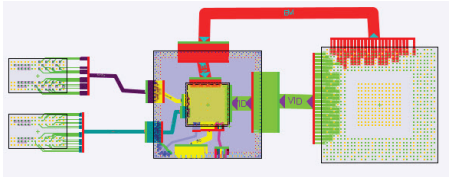
## Why Interface/Interconnect Planning and Optimization in CoWoS and InFO?

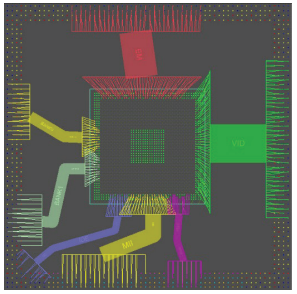
- Design in the context of chip, package, and board
- Reduce layer count of board and/or package
- Reduce overall turnaround time
- Improve signal and power integrity
- Reduce design margins

## Design Environment

- Core functionality with two design environments for CoWoS and InFO
  - OrbitIO design environment for hierarchical system-level exploration, pin creation, and optimization
  - Physical layout tools for implementation and refinement
    - Cadence® SiP Layout package layout tool for design layout and refinement
    - Allegro PCB layout environment
    - Innovus™ Implementation System or
    - Virtuoso custom design platform

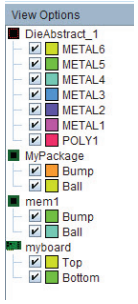


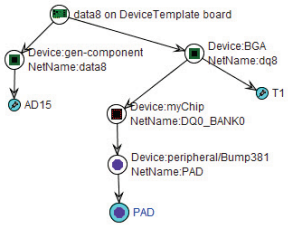


## Hierarchical Database

- Preserve technology, layer stack-up, and net names for each device in the hierarchy
- As signals traverse devices, net names may change
- Provide net graphing to easily see net throughout whole system

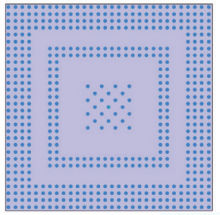


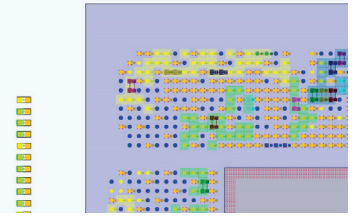

 

## Ball, Bump, and I/O Pad Ring Design

- Create or import a wide variety of standard or custom pin patterns and I/O pad rings

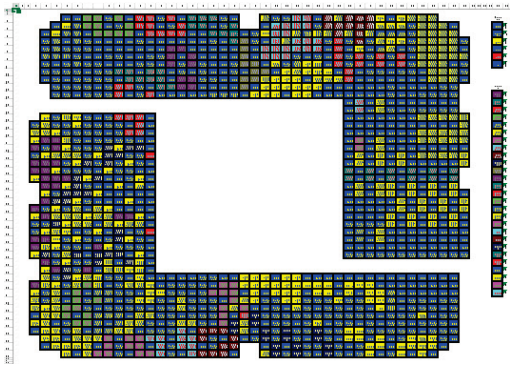


- Support LEF/DEF, .dra, .csv, die abstract, die/bga txt, .spd
- Create patterns of signal, power, and ground to guide net assignment



## Pin Optimization



- This is a key pathway design feature
- Start from known, fixed-pin configurations
  - Board component breakout endpoints
  - Known die IP blocks
  - Existing BGA footprints
- Optimize the placement of bumps or I/O drivers in a die based on route topology from a component on the PCB
  - If you have defined component breakouts on a PCB component, the ordering of the signals to the breakouts can drive signal sequence throughout the design
- Generate spreadsheet ball map for documentation and design review

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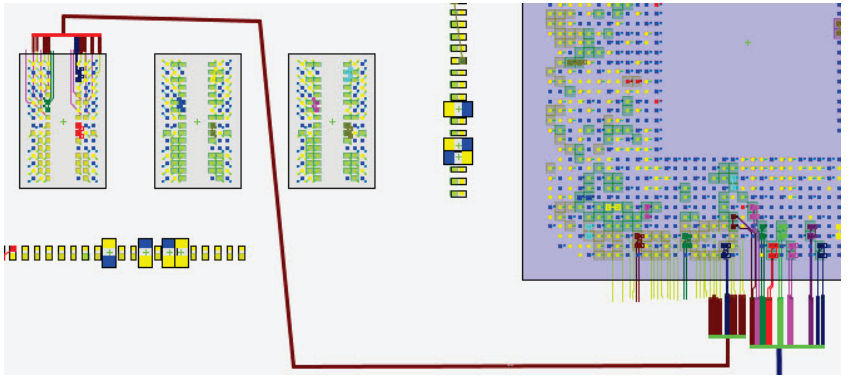
## Interconnect/Interface with Bundling



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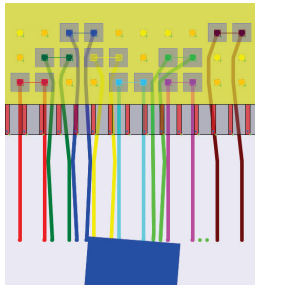
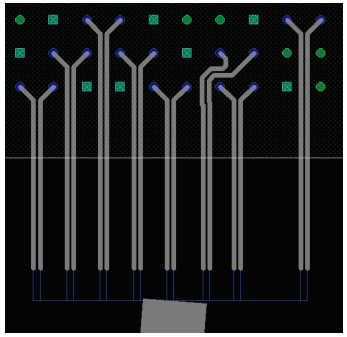
## Breakout Routing

- Die breakout
- Ball array break-in
- Ball array break-out (on PCB substrate)
- Enables accurate layer count estimations
- Follows differential pair settings
- Control wire spacing and width parameters
- Drives actual routing





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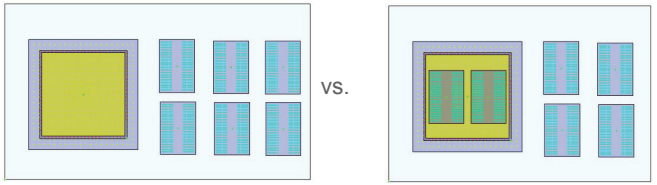
## Exploring System Topology Options

- Explore tradeoffs for various configurations
- Determine if a part should be on the board, in the package, or on an interposer
- Drag and drop components from one level of hierarchy to another



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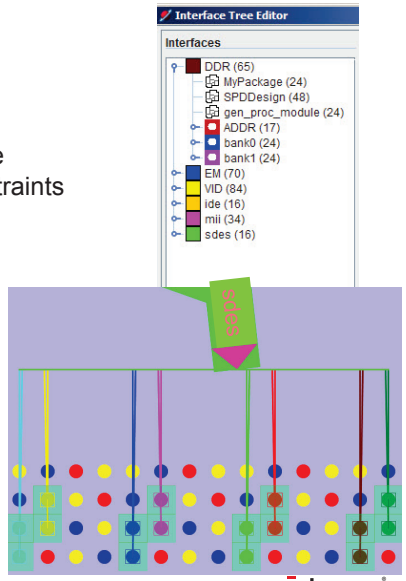
## Constraints

- Must keep it simple!
- Early stage doesn't deal with full-scale routing, so no need for full-scale constraints
- How much is enough?
- Interfaces—keep signals grouped according to function
- Width, spacing, differential pairs
- Interface definitions and diff pairs must transfer between tools



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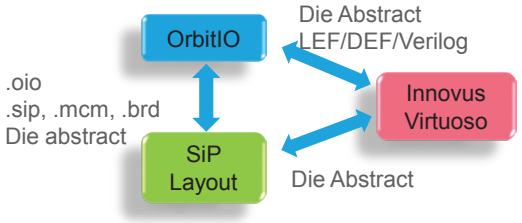
## Interoperability

- The hierarchical pathway design environment and the physical layout environments must efficiently talk with each other!
- Binary exchange between Cadence tools
  - Allegro PCB and Cadence SiP Layout read OrbitIO interconnect designer database directly
  - OrbitIO system planner reads .mcm, .pcb, and .sip files directly
  - Support other formats through .spd translation
- Die abstract is used to exchange die information between Innovus and Virtuoso design environments and system design and layout tools



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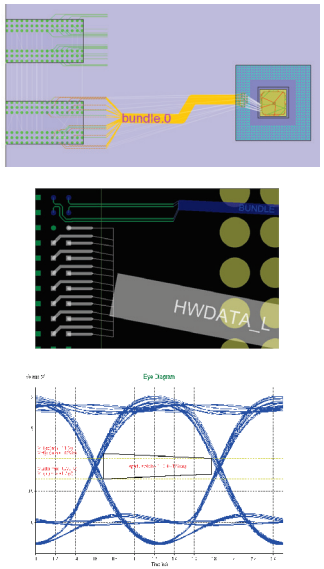
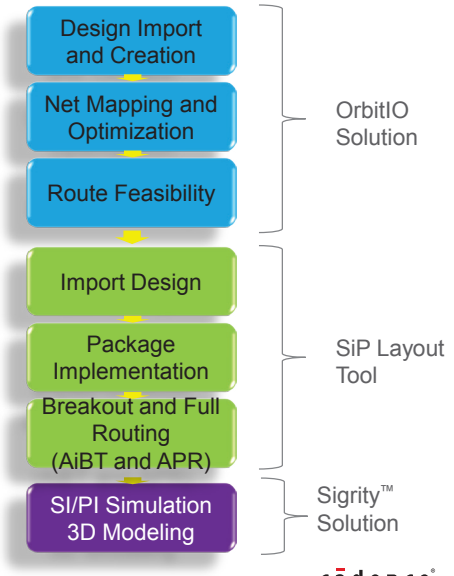
## Generic Flow for CoWoS and InFO



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## Conclusions

- Interface planning and optimization environment allows non-layout experts to design and optimize package and die pins
- Planning of breakouts further optimizes routability and reducing layer count
- Design from nothing and design from existing allows start of interconnect/interface planning early in the design flow
- Variant design flows provide greater visibility into all variants at once
- Reduce design costs by lowering layer count, shrinking design time, and providing greater predictability of meeting constraints in a broader design context

 

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